Remarks/Arguments

Examiner Howard Weiss is thanked for the continued thorough Search and Examination of the Subject Application for Patent.

Claims 1 and 8 have been amended to include the limitations that the potentials of the P well or wells can be set so that the overlap region or regions can be depleted of charge during the charge integration period and not depleted of charge carriers after the charge integration period has been completed. Claims 18, and 25 have been amended to include the limitations that the potentials of the N well or wells can be set so that the overlap region or regions can be depleted of charge during the charge integration period and not depleted of charge carriers after the charge integration period has been completed. The basis for these amendments to Claims 1, 8, 18, and 25 can be found in the Specification on page 6, lines13-22. These amendments are made at this time to answer the points raised by Examiner Weiss in the 35 USC 112, first paragraph, rejection of Claims 1-34. These amendments are made at this time to place the claims in better condition for appeal.

Reconsideration of the Rejection of Claims 1-34 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement is requested. Claims 1 and 8 have been amended to include the limitations that the potentials of the P well or wells can be set so that the overlap region or regions can be depleted of charge during the charge integration period and not depleted of charge carriers after the charge

integration period has been completed. Claims 18, and 25 have been amended to include the limitations that the potentials of the N well or wells can be set so that the overlap region or regions can be depleted of charge during the charge integration period and not depleted of charge carriers after the charge integration period has been completed. It is believed that, as amended, Claims 1-34 meet the requirements of 35 U.S.C. 112, first paragraph.

Reconsideration of the Rejection of Claims 1-17 under 35 U.S.C. 102(b) as being anticipated by Iwanami et al. (U.S. Pat. No. 4,906,856) is requested. Claims 1-17 are significantly different from the invention of Iwanami et al. for the following reasons. Claims 1-17 describe an active pixel sensor having an N well formed in a p type substrate, a P well formed in the N well, and a deep N well formed beneath the P well between the P well and the p type substrate, and an n type overlap region between the N well and the deep N well. Charge is accumulated by the deep N well during a charge integration period and the overlap region is used to isolate the deep N well from the N well during the charge integration period, by depleting the overlap region of charge carriers. The deep N well is connected to the N well after the charge integration period has been completed by supplying sufficient charge carriers to the overlap region. This allows the charge accumulated by the deep N well during the charge integration period to be transferred to the surface through the N well after the charge integration period has been completed. In the active pixel sensor of Claims 1-17 the deep N well is between the P well and the p type substrate. Claims 1-17 describe a vertical charge transfer device. The charges are accumulated in the deep N well during the charge integration period,

when the overlap region is depleted, and are transferred to the surface through the N well, when the overlap region is not depleted.

The invention of Iwanami et al. describes a bipolar photo transistor having a base 6, an emitter 9, a collector comprising an n type epitaxial region 3 and a collector region 10 formed in the n type epitaxial layer 3; and an N channel MOSFET having source and drain regions 8 and 8' formed in a p well 5. Both the bipolar photo transistor and the MOSFET are surface charge transfer devices, see Fig. 2a and column 2, lines 6-40. Both the base 6 of the photo transistor and the p well 5 of the MOSFET are formed in the n type epitaxial layer 3 which is formed on a p type substrate 1. All of the charge transfer activity takes place near the surface of the device. Iwanami et al. describe an n type built in layer 2 having a high impurity density selectively formed over the p type substrate 1. The n type epitaliax layer 3 is formed over the built in layer 2 and the p type substrate 1. The p type base region 6 for the photo transistor is formed in the n type epitaxial layer as is the p type well 5 for the MOSFET. P type isolation regions 4 are formed in the n type epitaxial layer 4 to isolate individual devices, see Fig. 2a and column 2, lines 6-16. The devices described by Iwanami et al. do not use charge depletion regions between different regions of the n type epitaxial layer and those skilled in the art would expect the devices to be designed so that charge depletion regions between different regions of the n type epitaxial layer would not occur.

Iwanami et al. describe surface charge transfer devices and do not describe vertical transfer devices. Iwanami et al. do not show or describe an overlap region which

can be depleted or not depleted in order to accumulate charge in a deep N well during a charge integration period, as is described in Claims 1-17. Since the n type epitaxial layer 3 are used for the collector of the bipolar photo transistor and the channel region for the MOSFET it would be expected by those skilled in the art that the device would be designed so that depletion regions in different regions of the n type epitaxial layer would not occur and are not described by Iwanami et al.. The n type built in layer 2 can not be isolated from the n type epitaxial layer 3 because the built in layer 2 is specifically formed with a high impurity density, see column 2, lines 9-13, which will work against carrier depletion in regions between the built in layer 2 and the n type epitaxial layer 3. Iwanami et al. do not describe regions below the surface region of the n type epitaxial layer which are capable of accumulating charge during a charge integration period.

I wanami et al. describe a P conductive substrate 1, an N type built-in-layer 2 of high impurity density, an N type epitaxial layer 3 formed over the built-in-layer, a P well 5 of an N channel MOS transistor, and a p type separating layer 4 formed to reach the P type substrate 1 from the surface of the surface of the n type epitaxial layer 3, see Fig. 2a and column 2, lines 6-20. It is believed that this structure described by Iwanami et al. is different from the active pixel sensor device having an N well formed in a p type epitaxial substrate, a P well formed in the N well, a deep N well formed in the p type epitaxial substrate beneath the P well, and an overlap region formed between the N well and the deep N well, described in Claims 1-17. Reconsideration of the Rejection of Claims 1-17 under 35 U.S.C. 102(b) as being anticipated by Iwanami et al., and allowance of Claims 1-17, are requested.

Reconsideration of the Rejection of Claims 18-34 under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (U.S. Pat. No. 6,023,293) is requested. Claims 18-34 are significantly different from the invention of Watanabe et al. for the following reasons. Claims 18-34 describe an active pixel sensor having an N well formed in a P well and a deep P well formed beneath the N well with an overlap region between the P well and the deep P well. Charge is accumulated by the deep P well during a charge integration period and transferred to the P well after the charge integration period has been completed. The overlap region is used to isolate the deep P well from the P well during the charge integration period by depleting the overlap region of charge carriers. The deep P well is connected to the P well after the charge integration period has been completed by not depleting the overlap region so that the charge accumulated by the deep P well during the charge integration period can be transferred to the surface through the P well after the charge integration period has been completed. Claims 18-34 describe a vertical charge transfer device. The charges are accumulated in the deep P well during the charge integration period, when the overlap region is depleted, and are transferred to the surface through the P well, when the overlap region is not depleted.

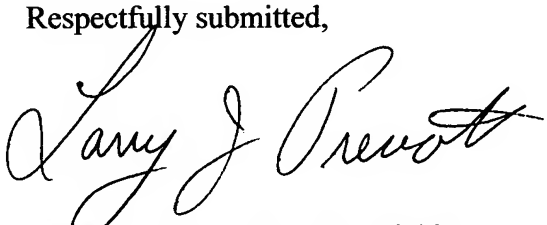
Watanabe et al. describe a solid state imaging device having a photoelectric conversion element which includes a transistor comprising a semiconductor region provided on a surface of a first semiconductor layer, a first gate region including a portion of the surface of the first semiconductor layer in which signal charges generated by photoelectric conversion are accumulated, a first gate electrode, a second gate region

formed on the portion of the first semiconductor layer adjacent to the first gate region, and a second gate electrode, see column 7, line 66 to column 8, line 23. In the invention of Watanabe et al. n^- wells are formed in a p type substrate and n^+ source and drain regions are formed in and at the surface of the n^- wells. A p^+ reset drain is formed at the surface of the p type substrate between the n^- wells. The photo signal is generated from charge flow affecting the potential of the n^+ source and reset is accomplished by charge flowing between the n^+ drain and the p^+ reset drain. All of the charge transfer takes place at the surface of the n^- wells or at the surface of the p type substrate between the n^- wells, see Fig. 18 and column 10, lines 21-65. All of the charge transfer takes place at the surface of the device and there is no charge flow from charges stored in a deep P well to the surface through a P well controlled by an overlap region which can be depleted to store charge and not depleted to transfer charge to the surface of the device, as is described in Claims 18-34. Since in the invention of Watanabe et al. the p type substrate separates the n^- wells and all charge flow is at the surface, those skilled in the art would not expect regions of the p type substrate which can be depleted of charge and are not described by Watanabe et al. Without regions of the p type substrate which can be depleted of charge the use a deep P well, a P well, and an overlap region between the P well and the deep P well which can be depleted or not depleted of charge carriers to control charge flow from the deep P well to the surface through the P well, as is described in Claims 18-34, is not described by Watanabe et al. nor suggested to those skilled in the art.

Claims 18-34 describe a P well formed in an n type epitaxial substrate, an N well formed in the P well, a deep P well formed in the n type epitaxial substrate beneath the N well, and an overlap region formed between the P well and the deep P well. Watanabe et al. do not describe an overlap region, as is described in Claims 18-34. Since Watanabe et al. describe a solid state imaging device which uses surface charge flow, Watanabe et al. would not be expected to want an overlap region which can readily be depleted of charge. Reconsideration of the Rejection of Claims 18-34 under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. and allowance of Claims 18-34 are requested.

It is requested that should Examiner Weiss not find that the Claims are now Allowable that the Examiner call the undersigned Agent at (845)-462-5363 to overcome any problems preventing allowance.

Respectfully submitted,



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